LC²MOS
Complete, 12-Bit Analog I/O System

AD7868

FEATURES

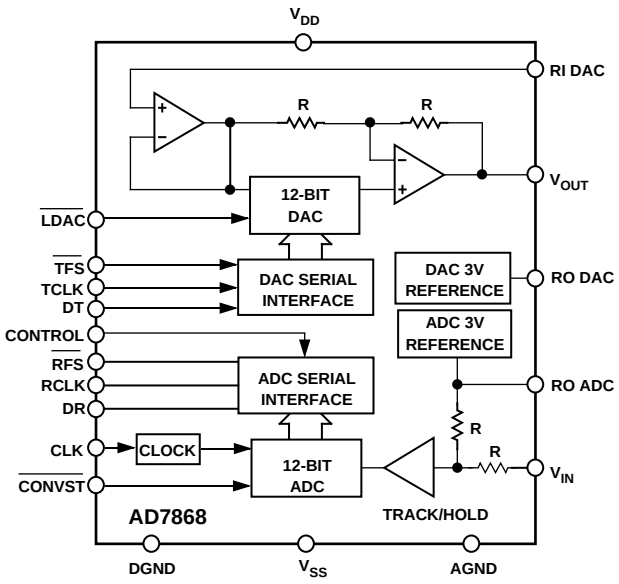
Complete 12-Bit I/O System, Comprising:
- **12-Bit ADC with Track/Hold Amplifier**
  - **83 kHz Throughout Rate**
  - **72 dB SNR**
- **12-Bit DAC with Output Amplifier**
  - **3 μs Settling Time**
  - **72 dB SNR**
- **On-Chip Voltage Reference**

Operates from ±5 V Supplies
Low Power – 130 mW typ
Small 0.3" Wide DIP

APPLICATIONS

Digital Signal Processing
Speech Recognition and Synthesis
Spectrum Analysis
High Speed Modems
DSP Servo Control

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7868 is a complete 12-bit I/O system containing a DAC and an ADC . The ADC is a successive approximation type with a track-and-hold amplifier having a combined throughput rate of 83 kHz. The DAC has an output buffer amplifier with a settling time of 3 μs to 12 bits. Temperature compensated 3 V buried Zener references provide precision references for the DAC and ADC.

Interfacing to both the DAC and ADC is serial, minimizing pin count and giving a small 24-pin package size. Standard control signals allow serial interfacing to most DSP machines. Asynchronous ADC conversion control and DAC updating is made possible with the $\overline{\text{CONVST}}$ and $\overline{\text{LDAC}}$ logic inputs.

The AD7868 operates from ±5 V power supplies, the analog input/output range of the ADC/DAC is ±3 V. The part is fully specified for dynamic parameters such as signal-to-noise ratio and harmonic distortion as well as traditional dc specifications.

The part is available in a 24-pin, 0.3" wide, plastic or hermetic dual-in-line package (DIP) and in a 28-pin, plastic SOIC package.

PRODUCT HIGHLIGHTS

1. Complete 12-Bit I/O System.
   The AD7868 contains a 12-bit ADC with a track-and-hold amplifier and a 12-bit DAC with output amplifier. Also included are separate on-chip voltage references for the DAC and the ADC.
2. Dynamic Specifications for DSP Users.
   In addition to traditional dc specifications, the AD7868 is specified for ac parameters including signal-to-noise ratio and harmonic distortion. These parameters along with important timing parameters are tested on every device.
3. Small Package.
   The AD7868 is available in a 24-pin DIP and a 28-pin SOIC package.

REV. B

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AD7868–SPECIFICATIONS

ADC SECTION

(V_{DD} = +5 V ± 5%, V_{SS} = –5 V ± 5%, AGND = DGND = 0 V, f_{CLK} = 2.0 MHz external. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A Version[1]	B Version[1]	T Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]					
Signal-to-Noise Ratio[3, 4] (SNR) @ +25°C	70	72	70	dB min	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 83 kHz
T_{MIN} to T_{MAX}	70	71	70	dB min	Typically 71.5 dB for 0 < V_{IN} < 41.5 kHz
Total Harmonic Distortion (THD)	–78	–78	–76	dB max	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 83 kHz Typically 71.5 dB for 0 < V_{IN} < 41.5 kHz
Peak Harmonic or Spurious Noise	–78	–78	–76	dB max	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 83 kHz Typically 71.5 dB for 0 < V_{IN} < 41.5 kHz
Intermodulation Distortion (IMD)					
Second Order Terms	–78	–78	–76	dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
Third Order Terms	–80	–80	–78	dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
Track/Hold Acquisition Time	2	2	2	µs max	
DC ACCURACY					
Resolution	12	12	12	Bits	
Minimum Resolution	12	12	12	Bits	No Missing Codes Are Guaranteed
Integral Nonlinearity	±12	±12	±12	LSB typ	
Integral Nonlinearity		±1	±1	LSB max	
Differential Nonlinearity	±0.9	±0.9	±0.9	LSB max	
Bipolar Zero Error	±5	±5	±5	LSB max	
Positive Gain Error[5]	±5	±5	±5	LSB max	
Negative Gain Error[5]	±5	±5	±5	LSB max	
ANALOG INPUT					
Input Voltage Range	±3	±3	±3	Volts	
Input Current	±1	±1	±1	mA max	
REFERENCE OUTPUT[6]					
RO ADC @ +25°C	2.99/3.01	2.99/3.01	2.99/3.01	V min/V max	
RO ADC TC	±25	±25	±25	ppm/°C typ	
RO ADC TC		±40	±50	ppm/°C max	
Reference Load Sensitivity (ΔRO ADC vs. ΔI)	–1.5	–1.5	–1.5	mV max	Reference Load Current Change (0 µA–500 µA), Reference Load Should Not Be Changed During Conversion
LOGIC INPUTS ($\overline{CONVST}$, CLK, CONTROL)					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	µA max	V_{IN} = 0 V to V_{DD}
Input Current[7] (CONTROL Input Only)	±10	±10	±10	µA max	V_{IN} = V_{SS} to DGND
Input Capacitance, C_{IN}[8]	10	10	10	pF max	
LOGIC OUTPUTS					
DR, $\overline{RFS}$ Outputs					
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA, Pull-Up Resistor = 4.7 kΩ
RCLK Output					
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 2.6 mA, Pull-Up Resistor = 2 kΩ
DR, $\overline{RFS}$, RCLK Outputs					
Floating-State Leakage Current	±10	±10	±10	µA max	
Floating-State Output Capacitance[8]	15	15	15	pF max	
CONVERSION TIME					
External Clock	10	10	10	µs max	
Internal Clock	10	10	10	µs max	The Internal Clock Has a Nominal Value of 2.0 MHz
POWER REQUIREMENTS					For Both DAC and ADC
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
V_{SS}	–5	–5	–5	V nom	±5% for Specified Performance
I_{DD}	22	22	25	mA max	Cumulative Current from the Two V_{DD} Pins
I_{SS}	12	12	13	mA max	Cumulative Current from the Two V_{SS} Pins
Total Power Dissipation	170	170	190	mW max	Typically 130 mW

NOTES

[1]Temperature ranges are as follows: A/B Versions, –40°C to +85°C; T Version, –55°C to +125°C.

[2]V_{IN} = ±3 V

[3]SNR calculation includes distortion and noise components.

[4]SNR degradation due to asynchronous DAC updating during conversion is 0.1 dB typ.

[5]Measured with respect to internal reference.

[6]For capacitive loads greater than 50 pF a series resistor is required (see INTERNAL REFERENCE section).

[7]Tying the CONTROL input to V_{DD} places the device in a factory test mode where normal operation is not exhibited.

[8]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

DAC SECTION

(V_{DD} = +5 V ± 5%, V_{SS} = –5 V ± 5%, AGND = DGND = 0 V, RI DAC = +3 V and decoupled as shown in Figure 2, V_{OUT} Load to AGND; R_L = 2 kΩ, C_L = 100 pF. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A Version[1]	B Version[1]	T Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]					
Signal-to-Noise Ratio[3] (SNR) @ +25°C	70	72	70	dB min	V_{OUT} = 1 kHz Sine Wave, f_{SAMPLE} = 83 kHz
T_{MIN} to T_{MAX}	70	71	70	dB min	Typically 71.5 dB at +25°C for 0 < V_{OUT} < 20 kHz[4]
Total Harmonic Distortion (THD)	–78	–78	–76	dB max	V_{OUT} = 1 kHz Sine Wave, f_{SAMPLE} = 83 kHz
					Typically –84 dB at +25°C for 0 < V_{OUT} < 20 kHz[4]
Peak Harmonic or Spurious Noise	–78	–78	–76	dB max	V_{OUT} = 1 kHz Sine Wave, f_{SAMPLE} = 83 kHz
					Typically –84 dB at +25°C for 0 < V_{OUT} < 20 kHz[4]
DC ACCURACY					
Resolution	12	12	12	Bits	
Integral Nonlinearity	±1/2	±1/2	±1/2	LSB typ	
Integral Nonlinearity		±1	±1	LSB max	
Differential Nonlinearity	±0.9	±0.9	±0.9	LSB max	Guaranteed Monotonic
Bipolar Zero Error	±5	±5	±5	LSB max	
Positive Full-Scale Error[5]	±5	±5	±5	LSB max	
Negative Full-Scale Error[5]	±5	±5	±5	LSB max	
REFERENCE OUTPUT[6]					
RO ADC @ +25°C	2.99/3.01	2.99/3.01	2.99/3.01	V min/V max	
RO ADC TC	±25	±25	±25	ppm/°C typ	
RO ADC TC		±40	±50	ppm/°C max	
Reference Load Change (ΔRO DAC vs. ΔI)	–1.5	–1.5	–1.5	mV max	Reference Load Current Change (0–500 μA)
REFERENCE INPUT					
RI DAC Input Range	2.85/3.15	2.85/3.15	2.85/3.15	V min/V max	3 V ± 5%
Input Current	1	1	1	μA max	
LOGIC INPUTS ($\overline{LDAC}$, $\overline{TFS}$, TCLK, DT)					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[7]	10	10	10	pF max	
ANALOG INPUT					
Output Voltage Range	±3	±3	±3	V nom	
dc Output Impedance	0.3	0.3	0.3	Ω typ	
Short-Circuit Current	20	20	20	mA typ	
AC CHARACTERISTICS[7]					
Voltage Output Settling-Time					Settling Time to Within ±1/2 LSB of Final Value
Positive Full-Scale Change	3	3	3	μs max	Typically 2 μs
Negative Full-Scale Change	3	3	3	μs max	Typically 2.5 μs
Digital-to-Analog Glitch Impulse	10	10	10	nV secs typ	DAC Code Change All 1s to All 0s
Digital Feedthrough	2	2	2	nV secs typ	
V_{IN} to V_{OUT} Isolation	100	100	100	dB typ	V_{IN} = ±3 V, 41.5 kHz Sine Wave
POWER REQUIREMENTS	As per ADC Section				

NOTES

[1]Temperature ranges are as follows: A/B Versions, –40°C to +85°C; T Version, –55°C to +125°C.

[2]V_{OUT} (pk–pk) = ±3 V.

[3]SNR calculation includes distortion and noise components.

[4]Using external sample and hold.

[5]Measured with respect to RI DAC and includes bipolar offset error.

[6]For capacitive loads greater than 50 pF a series resistor is required (see INTERNAL REFERENCE section).

[7]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature Range	SNR	Relative Accuracy (LSB)	Package Option*
AD7868AN	–40°C to +85°C	70 dB	±1/2 typ	N-24
AD7868AQ	–40°C to +85°C	70 dB	±1/2 typ	Q-24
AD7868BN	–40°C to +85°C	72 dB	±1 max	N-24
AD7868BQ	–40°C to +85°C	72 dB	±1 max	Q-24
AD7868AR	–40°C to +85°C	70 dB	±1/2 typ	R-28
AD7868BR	–40°C to +85°C	72 dB	±1 max	R-28

*N = Plastic DIP; Q = Cerdip; R = SOIC (Small Outline IC).

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +5 V ± 5%, V_{SS} = –5 V ± 5%, AGND = DGND = 0 V)

Parameter	Limit at T_{MIN}, T_{MAX} (A, B Versions)	Limit at T_{MIN}, T_{MAX} (T Version)	Units	Conditions/Comments
ADC TIMING				
t_1	50	50	ns min	$\overline{\text{CONVST}}$ Pulse Width
t_2[3]	440	440	ns min	RCLK Cycle Time, Internal Clock
t_3	100	100	ns min	$\overline{\text{RFS}}$ to RCLK Falling Edge Setup Time
t_4	20	20	ns min	RCLK Rising Edge to $\overline{\text{RFS}}$
	100	100	ns max	
t_5[4]	155	155	ns max	RCLK to Valid Data Delay, C_L = 35 pF
t_6	4	4	ns min	Bus Relinquish Time after RCLK
	100	100	ns max	
t_{13}[5]	2 RCLK +200 to 3 RCLK + 200	2 RCLK +200 to 3 RCLK + 200	ns typ	$\overline{\text{CONVST}}$ to $\overline{\text{RFS}}$ Delay
DAC TIMING				
t_7	50	50	ns min	$\overline{\text{TFS}}$ to TCLK Falling Edge
t_8	75	100	ns min	TCLK Falling Edge to $\overline{\text{TFS}}$
t_9[6]	150	200	ns min	TCLK Cycle Time
t_{10}	30	40	ns min	Data Valid to TCLK Setup Time
t_{11}	75	100	ns min	Data Valid to TCLK Hold Time
t_{12}	40	40	ns min	$\overline{\text{LDAC}}$ Pulse Width

NOTES

[1]Timing specifications are sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]Serial timing is measured with a 4.7 kΩ pull-up resistor on DR and $\overline{\text{RFS}}$ and a 2 kΩ pull-up resistor on RCLK . The capacitance on all three output is 35 pF.

[3]When using internal clock, RCLK mark/space ratio (measured from a voltage level of 1.6 V) range is 40/60 to 60/40. For external clock, RCLK mark/space ratio = external clock mark/space ratio.

[4]DR will drive higher capacitance loads but this will add to t_5 since it increases the external RC time constant (4.7 kΩ/C_L) and hence the time to reach 2.4 V.

[5]Time 2 RCLK to 3 RCLK depends on conversion start to ADC clock synchronization.

[6]TCLK mark/space ratio is 40/60 to 60/40.

ABSOLUTE MAXIMUM RATINGS*

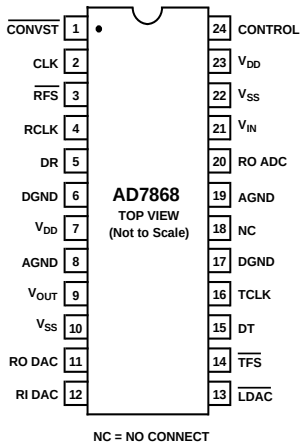
(T_A = +25°C unless otherwise noted)

V_{DD} to AGND ..... –0.3 V to +7 V
V_{SS} to AGND ..... +0.3 V to –7 V
AGND to DGND ..... –0.3 V to V_{DD} +0.3 V
V_{OUT} to AGND ..... V_{SS} to V_{DD}
V_{IN} to AGND ..... V_{SS} –0.3 V to V_{DD} + 0.3 V
RO ADC to AGND ..... –0.3 V to V_{DD} + 0.3 V
RO DAC to AGND ..... –0.3 V to V_{DD} + 0.3 V
RI DAC to AGND ..... –0.3 V to V_{DD} + 0.3 V
Digital Inputs to AGND ..... –0.3 V to V_{DD} + 0.3 V
Digital Outputs to AGND ..... –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
A, B Versions ..... –40°C to +85°C
T Version ..... –55°C to +125°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 secs) ..... +300°C
Power Dissipation (Any Package) to +75°C ..... 450 mW
Derates above +75°C by ..... 10 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

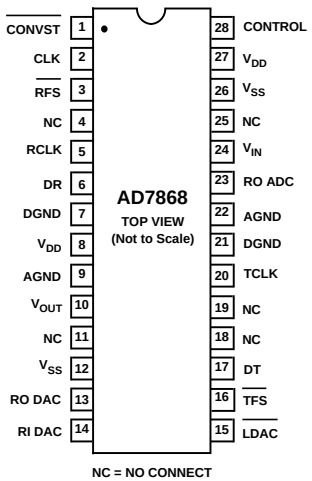
PIN CONFIGURATIONS

DIP



NC = NO CONNECT

SOIC



NC = NO CONNECT

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7868 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTION

DIP Pin Number	Mnemonic	Function
POWER SUPPLY		
7 & 23	V_{DD}	Positive Power Supply, 5 V ± 5%. Both V_{DD} pins must be tied together.
10 & 22	V_{SS}	Negative Power Supply, –5 V ± 5%. Both V_{SS} pins must be tied together.
8 & 19	AGND	Analog Ground. Both AGND pins must be tied together.
6 &17	DGND	Digital Ground. Both DGND pins must be tied together.
ANALOG SIGNAL AND REFERENCE		
21	V_{IN}	ADC Analog Input. The ADC input range is ±3 V.
9	V_{OUT}	Analog Output Voltage from DAC. This output comes from a buffer amplifier. The range is bipolar, ±3 V with RI DAC = +3 V.
20	RO ADC	Voltage Reference Output. The internal ADC 3 V reference is provided at this pin. This output may be used as a reference for the DAC by connecting it to the RI DAC input. The external load capability of this reference is 500 μA.
11	RO DAC	DAC Voltage Reference Output. This is one of two internal voltage references. To operate the DAC with this internal reference, RO DAC should be connected to RI DAC. The external load capability of the reference is 500 μA.
12	RI DAC	DAC Voltage Reference Input. The voltage reference for the DAC must be applied to this pin. It is internally buffered before being applied to the DAC. The nominal reference voltage for correct operation of the AD7868 is 3 V.
ADC INTERFACE AND CONTROL		
2	CLK	Clock Input. An external TTL-compatible clock may be applied to this input. Alternatively, tying pin to V_{SS} enables the internal laser-trimmed oscillator.
3	$\overline{\text{RFS}}$	Receive Frame Synchronization, Logic Output. This is an active low open-drain output which provides a framing pulse for serial data. An external 4.7 kΩ pull-up resistor is required on $\overline{\text{RFS}}$.
4	RCLK	Receive Clock, Logic Output. RCLK is the gated serial clock output which is derived from the internal or external ADC clock. If the CONTROL input is at V_{SS} the clock runs continuously. With the CONTROL input at DGND the RCLK output is gated off (three-stated) after serial transmission is complete. RCLK is an open-drain output and requires an external 2 kΩ pull-up resistor.
5	DR	Receive Data, Logic Output. This is an open-drain data output used in conjunction with $\overline{\text{RFS}}$ and RCLK to transmit data from the ADC. Serial data is valid on the falling edge of RCLK when $\overline{\text{RFS}}$ is low. An external 4.7 kΩ resistor is required on the DR output.
1	$\overline{\text{CONVST}}$	Convert Start, Logic Input. A low to high transition on this input puts the track-and-hold amplifier into the hold mode and starts an ADC conversion. This input in asynchronous to the CLK input.
24	CONTROL	Control, Logic Input. With this pin at 0 V, the RCLK is noncontinuous. With this pin at –5 V, the RCLK is continuous. Note, tying this pin to V_{DD} places the part in a factory test mode where normal operation is not exhibited.
DAC INTERFACE AND CONTROL		
14	$\overline{\text{TFS}}$	Transmit Frame Synchronization, Logic Input. This is a frame or synchronization signal for the DAC with serial data expected after the falling edge of this signal.
15	DT	Transmit Data, Logic Input. This is the data input which is used in conjunction with $\overline{\text{TFS}}$ and TCLK to transfer serial data to the input latch.
16	TCLK	Transmit Clock, Logic Input. Serial data bits are latched on the falling edge of TCLK when $\overline{\text{TFS}}$ is low.
13	$\overline{\text{LDAC}}$	Load DAC, Logic Input. A new word is transferred into the DAC latch from the input latch on the falling edge of this signal.
18	NC	No Connect.

CONVERTER DETAILS

The AD7868 is a complete 12-bit I/O port, the only external components required for normal operation are pull-up resistors for the ADC data outputs and power supply decoupling capacitors. It is comprised of a 12-bit successive approximation ADC with a track/hold amplifier, a 12-bit DAC with a buffered output and two 3 V buried Zener references, a clock oscillator and control logic.

ADC CLOCK

The AD7868 has an internal clock oscillator which can be used for the ADC conversion procedure. The oscillator is enabled by tying the CLK input to V_{SS}. The oscillator in laser trimmed at the factory to give a conversion time of between 8.5 and 10 μs. The mark/space ratio can vary from 40/60 to 60/40. Alternatively, an external TTL compatible clock may be applied to this input. The allowable mark/space ratio of an external clock is 40/60 to 60/40. RCLK is a clock output, used for the serial interface. This output is derived directly from the ADC clock source and can be switched off at the end of conversion with the CONTROL input.

ADC CONVERSION TIMING

The conversion time for both external clock and continuous internal clock can vary from 19 to 20 rising clock edges depending on the conversion start to ADC clock synchronization. If a conversion is initiated within 30 ns prior to a rising edge of the ADC clock, the conversion time will consist of 20 rising clock edges, i.e., 9.5 μs conversion time. For noncontinuous internal clock, the conversion time is always 19 rising clock edges.

ADC TRACK-AND-HOLD AMPLIFIER

The track-and-hold amplifier on the analog input of the AD7868 allows the ADC to accurately convert an input sine wave of 6 V peak–peak amplitude to 12-bit accuracy. The input impedance is typically 9 kΩ, an equivalent circuit is shown in Figure 1. The input bandwidth of the track/hold amplifier is much greater than the Nyquist rate of the ADC, even when the ADC is operated at its maximum throughput rate. The 0.1 dB cutoff frequency occurs typically at 500 kHz. The track/hold amplifier acquires an input signal to 12-bit accuracy in less than 2 μs.

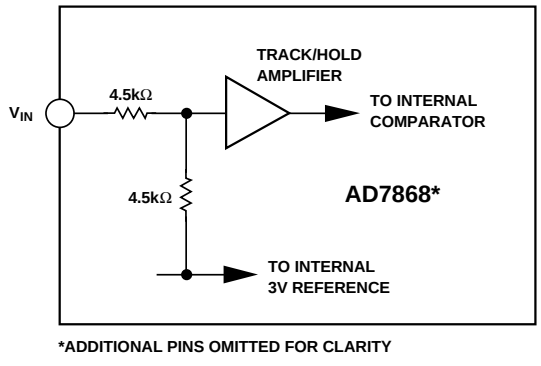


Figure 1. ADC Analog Input

The overall throughput rate is equal to the conversion time plus the track/hold amplifier acquisition time. For a 2.0 MHz input clock the throughput time is 12 μs max.

The operation of the track/hold amplifier is essentially transparent to the user. The track/hold amplifier goes from its track mode to its hold mode at the start of conversion on the rising edge of $\overline{\text{CONVST}}$.

INTERNAL REFERENCES

The AD7868 has two on-chip temperature compensated buried Zener references which are factory trimmed to 3 V ± 10 mV. One reference provides the appropriate biasing for the ADC, while the other is available as a reference of the DAC. Both reference outputs are available (labeled RO DAC and RO ADC) and are capable of providing up to 500 μA to an external load.

The DAC input reference (RI DAC) can be stored externally or connected to any of the two on-chip references. Applications requiring good full-scale error matching between the DAC and the ADC should use the ADC reference as shown in Figure 4.

The maximum recommended capacitance on either of the reference output pins for normal operation is 50 pF. If either of the reference outputs is required to drive a capacitive load greater than 50 pF, then a 200 Ω resistor must be placed in series with the capacitive load. The addition of decoupling capacitors, 10 μF in parallel with 0.1 μF, as shown in Figure 2, improves noise performance. The improvement in noise performance can be seen from the graph in Figure 3. Note, this applies for the DAC output only; reference decoupling components do not affect ADC performance. So, a typical application will have just the DAC reference source decoupled with the other one open circuited.

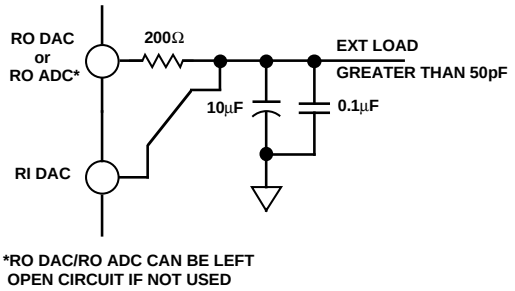


Figure 2. Reference Decoupling Circuitry

DAC OUTPUT AMPLIFIER

The output from the voltage-mode DAC is buffered by a noninverting amplifier. The buffer amplifier is capable of developing ±3 V across 2 kΩ and 100 pF load to ground and can produce 6 V peak-to-peak sine wave signals to a frequency of 20 kHz. The output is updated on the falling edge of the $\overline{\text{LDAC}}$ input. The output voltage settling time, to within 1/2 LSB of its final value, is typically less than 2 μs.

The small signal (200 mV p-p) bandwidth of the output buffer amplifier is typically 1 MHz. The output noise from the amplifier is low with a figure of 30 nV/$\sqrt{\text{Hz}}$ at a frequency of 1 kHz. The broadband noise from the amplifier exhibits a typical peak-to-peak figure of 150 μV for a 1 MHz output bandwidth. Figure 3 shows a typical plot of noise spectral density versus frequency for the output buffer amplifier and for either of the on-chip references.

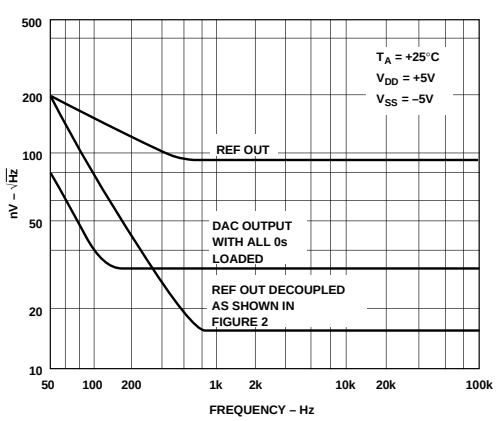


Figure 3. Noise Spectral Density vs. Frequency

INPUT/OUTPUT TRANSFER FUNCTIONS

A bipolar circuit for the AD7868 is shown in Figure 4. The analog input/output voltage range of the AD7868 is ±3 V. The designed code transitions for the ADC occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSB, 5/2 LSB . . . FS – 3/2 LSBs). The input/output code is 2s complement binary with 1 LSB = FS/4096 = 1.46 mV. The ideal transfer function is shown in Figure 5.

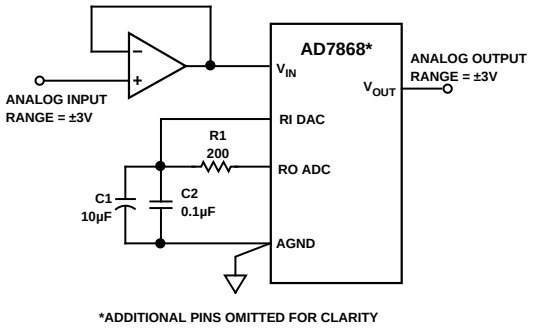


Figure 4. AD7868 Basic Bipolar Operation Using RO ADC as a Reference Input for the DAC

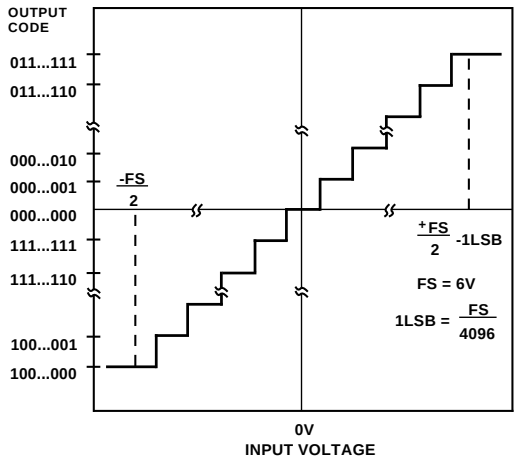


Figure 5. AD7868 Input/Output Transfer Function

OFFSET AND FULL-SCALE ADJUSTMENT

In most digital signal processing (DSP) applications, offset and full-scale errors have little or no effect on system performance. Offset error can always be eliminated in the analog domain by ac coupling. Full-scale errors do not cause problems as long as the input signal is within the full dynamic range of the ADC. For applications which require that the input signal range match the full analog input dynamic range of the ADC, offset and full-scale errors have to be adjusted to zero.

ADC ADJUSTMENT

Figure 6 has signal conditioning at the input and output of the AD7868 for trimming the end points of the transfer functions of both the ADC and the DAC. Offset error must be adjusted before full-scale error. For the ADC, this is achieved by trimming the offset of A1 while the input voltage, V1, is 1/2 LSB below ground. The trim procedure is as follows: apply a voltage of –0.73 mV (–1/2 LSB) at V1 in Figure 6 and adjust the offset voltage of A1 until the ADC output code flickers between 1111 1111 1111 (FFF HEX) and 0000 0000 0000 (000 HEX).

ADC gain error can be adjusted at either the first code transition (ADC negative full scale) or the last code transition (ADC positive full scale). The trim procedures for both cases are as follows (see Figure 6).

ADC Positive Full-Scale Adjustment

Apply a voltage of 2.9978 V (FS/2 – 3/2 LSBs) at V1. Adjust R2 until the ADC output code flickers between 0111 1111 1110 (7FE HEX) and 0111 1111 1111 (7FF HEX).

ADC Negative Full-Scale Adjustment

Apply a voltage of –2.9993 V (–FS/2 + 1/2 LSB) at V1 and adjust R2 until the ADC output code flickers between 1000 0000 0000 (800 HEX) and 1000 0000 0001 (801 HEX).

DAC ADJUSTMENT

Op amp A2 is included in Figure 6 for the DAC transfer function adjustment. Again offset must be adjusted before full scale. To adjust offset: load the DAC with 0000 0000 0000 (000 HEX) and trim the offset of A2 to 0 V. As with the ADC adjustment, gain error can be adjusted at either the first code transition (DAC negative full scale) or the last code transition (DAC positive full scale). The trim procedures for both cases are as follows:

DAC Positive Full-Scale Adjustment

Load the DAC with 0111 1111 1111 (7FF HEX) and adjust R7 until the op amp output voltage is equal to 2.9985 V, (FS/2 – 1 LSB).

DAC Negative Full-Scale Adjustment

Load the DAC with 1000 0000 0000 (800 HEX) and adjust R7 until the op amp output voltage is equal to 3.0 V (–FS/2).

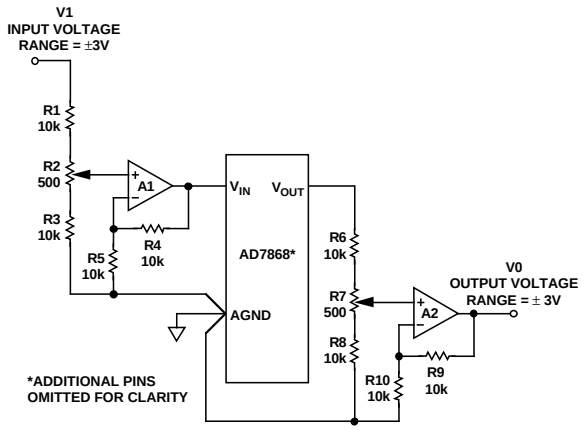


Figure 6. AD7868 with Input/Output Adjustment

TIMING AND CONTROL

Communication with the AD7868 is managed by 6 dedicated pins. These consist of separate serial clocks, word framing or strobe pulses and data signals for both receiving and transmitting data. Conversion starts and DAC updating are controlled by two digital inputs; $\overline{\text{CONVST}}$ and $\overline{\text{LDAC}}$. These inputs can be asserted independently of the microprocessor by an external timer when precise sampling intervals are required. Alternatively, the $\overline{\text{LDAC}}$ and $\overline{\text{CONVST}}$ can be driven from a decoded address bus allowing the microprocessor control over conversion start and DAC updating as well as data communication to the AD7868.

ADC Timing

Conversion control is provided by the $\overline{\text{CONVST}}$ input. A low to high transition on $\overline{\text{CONVST}}$ input starts conversion and drives the track/hold amplifier into its hold mode. Serial data then becomes available while conversion is in progress. The corresponding timing diagram is shown in Figure 7. The word length is 16 bits; 4 leading zeros, followed by the 12-bit conversion result starting with the MSB. The data is synchronized to the serial clock output (RCLK) and is framed by the serial strobe ($\overline{\text{RFS}}$). Data is clocked out on a low to high transition of the serial clock and is valid on the falling edge of this clock while the $\overline{\text{RFS}}$ output is low. $\overline{\text{RFS}}$ goes low at the start of conversion and the first serial data bit (which is the first leading zero) is valid on the first falling edge of RCLK. All the ADC serial lines are open-drain outputs and require external pull-up resistors.

The serial clock out is derived from the ADC master clock source which may be internal or external. Normally, RCLK is required during the serial transmission only. In these cases it can be shut down (i.e., placed into high impedance) at the end of conversion to allow multiple ADCs to share a common serial bus. However, some serial systems (e.g., TMS32020) require a serial clock which runs continuously. Both options are available on the AD7868 ADC. With the CONTROL input at 0 V, RCLK is noncontinuous and when it is at –5 V, RCLK is continuous.

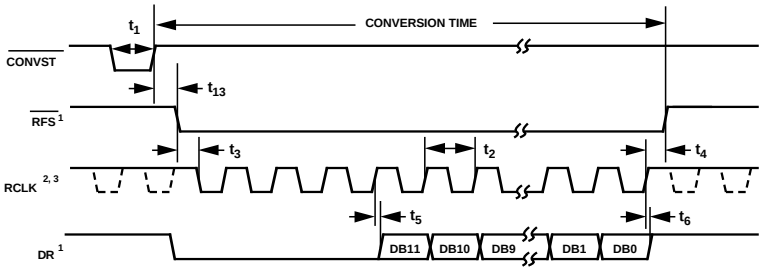
DAC Timing

The AD7868 DAC contains two latches, an input latch and a DAC latch. Data must be loaded to the input latch under the control of the TCLK, $\overline{\text{TFS}}$ and DT serial logic inputs. Data is then transferred from the input latch to the DAC latch under the control of the $\overline{\text{LDAC}}$ signal. Only the data in the DAC latch determines the analog output of the AD7868.

Data is loaded to the input latch under control of TCLK, $\overline{\text{TFS}}$ and DT. The AD7868 DAC expects a 16-bit stream of serial data on its DT input. Data must be valid on the falling edge of TCLK. The $\overline{\text{TFS}}$ input provides the frame synchronization signal which tells the AD7868 DAC that valid serial data will be available for the next 16 falling edges of TCLK. Figure 8 shows the timing diagram for the serial data format.

Although 16 bits of data are clocked into the input latch, only 12 bits are transferred into the DAC latch. Therefore, 4 bits in the stream are don't cares since their value does not affect the DAC latch data. The bit positions are 4 don't cares followed by the 12-bit DAC data starting with the MSB.

The $\overline{\text{LDAC}}$ signal controls the transfer of data to the DAC latch. Normally, data is loaded to the DAC latch on the falling edge of $\overline{\text{LDAC}}$. However, if $\overline{\text{LDAC}}$ is held low, then serial data is loaded to the DAC latch on the sixteenth falling edge of TCLK. If $\overline{\text{LDAC}}$ goes low during the loading of serial data to the input latch, no DAC latch update takes place on the falling edge of $\overline{\text{LDAC}}$. If $\overline{\text{LDAC}}$ stays low until the serial transfer is completed, then the update takes place on the sixteenth falling edge of TCLK. If $\overline{\text{LDAC}}$ returns high before the serial data transfer is completed, no DAC latch update takes place.



NOTES
[1]EXTERNAL 4.7k Ω PULL-UP RESISTOR
[2]EXTERNAL 2k Ω PULL-UP RESISTOR
[3]CONTINUOUS RCLK (DASHED LINE) WHEN THE CONTROL INPUT = –5V AND NONCONTINUOUS WHEN THE CONTROL INPUT = 0V

Figure 7. ADC Control Timing Diagram

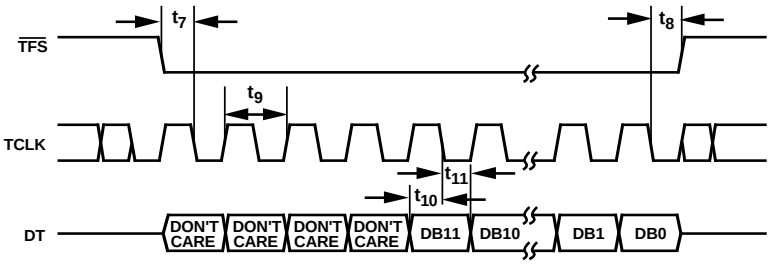


Figure 8. DAC Control Timing Diagram

AD7868 DYNAMIC SPECIFICATIONS

The AD7868 is specified and 100% tested for dynamic performance specifications as well as traditional dc specifications such as integral and differential nonlinearity. These ac specifications are required for signal processing applications such as speech recognition, spectrum analysis, and high-speed modems. These applications require information on the converter's effect on the spectral content of the input signal. Hence, the parameters for which the AD7868 is specified include SNR, harmonic distortion and peak harmonics. These terms are discussed in more detail in the following sections.

Signal-to-Noise Ratio (SNR)

SNR is the measured signal-to-noise ratio at the output of the ADC or DAC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency (fs/2) excluding dc. SNR is dependent upon the number of levels used in the quantization process; the more levels, the smaller the quantization noise. The theoretical signal-to-noise ratio for a sine wave input is given by

$$SNR = (6.02N + 1.76)\ dB \quad (1)$$

where N is the number of bits. Thus for an ideal 12-bit converter, SNR = 74 dB.

Effective Number of Bits

The formula given in Equation 1 relates the SNR to the number of bits. Rewriting the formula, as in Equation 2, it is possible to get a measure of performance expressed in effective number of bits (N).

$$N = \frac{SNR - 1.76}{6.02} \quad (2)$$

The effective number of bits for a device can be calculated directly from its measured SNR.

Harmonic Distortion

Harmonic distortion is the ratio of the rms sum of harmonics to the fundamental. For the AD7868, total harmonic distortion (THD) is defined as

$$THD = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through to the sixth harmonic. The THD is also derived from the FFT plot of the ADC or DAC output spectrum.

ADC Testing

The output spectrum from the ADC is evaluated by applying a sine-wave signal of very low distortion to the V_{IN} input which is sampled at an 83 kHz sampling rate. A Fast Fourier Transform (FFT) plot is generated from which the SNR data can be obtained. Figure 9 shows a typical 2048 point FFT plot of the AD7868BQ ADC with an input signal of 10 kHz and a sampling frequency of 83 kHz. The SNR obtained from this graph is 73 dB. It should be noted that the harmonics are taken into account when calculating the SNR.

Figure 10 shows a typical plot of effective number of bits versus frequency for an AD7868BQ with a sampling frequency of 83 kHz. The effective number of bits typically falls between 11.7 and 11.85 corresponding to SNR figures of 72.2 and 73.1 dB.

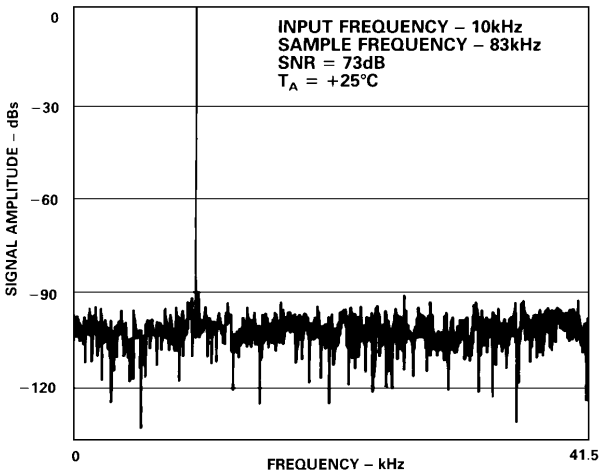


Figure 9. AD7868, ADC FFT Plot

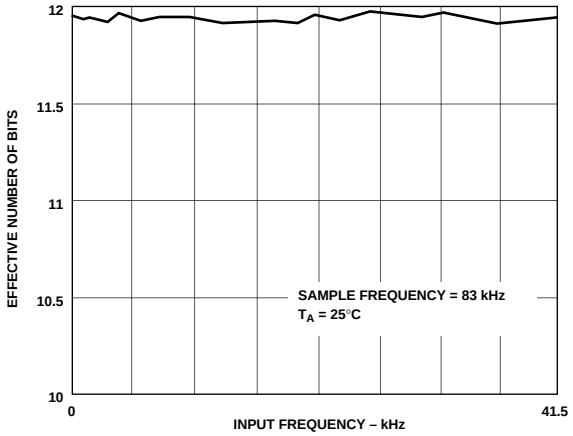


Figure 10. Effective Number of Bits vs. Frequency for the ADC

DAC Testing

A simplified diagram of the method used to test the dynamic performance specifications of the DAC is outlined in Figure 11. Data is loaded to the DAC under control of the microcontroller and associated logic. The output of the DAC is applied to a 9th order low-pass filter whose cutoff frequency corresponds to the Nyquist limit. The output of the filter is in turn applied to a 16-bit accurate digitizer. This digitizes the signal and the microcontroller generates an FFT plot from which the dynamic performance of the DAC can be evaluated.

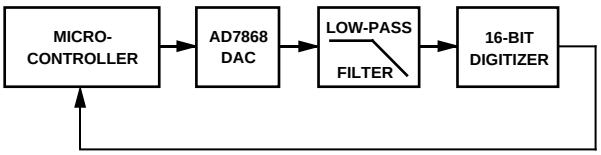


Figure 11. AD7868 DAC Dynamic Performance Test Circuit

The digitizer sampling is synchronized with the DAC update rate to ease FFT calculations. The digitizer samples the DAC output after the output has settled to its new value. Therefore, if the digitizer were to sample the output directly it would effectively be sampling a dc value each time. As a result, the dynamic performance of the DAC would not be measured correctly. Using the digitizer directly on the DAC output would give better results than the actual performance of the DAC. Using a filter between the DAC and the digitizer means that the digitizer samples a continuously moving signal and the true dynamic performance of the AD7868 DAC output is measured.

Figure 12 shows a typical 2048 point Fast Fourier Transform plot for the AD7868 DAC with an update rate of 83 kHz and an output frequency of 1 kHz. The SNR obtained from the graph is 73 dBs.

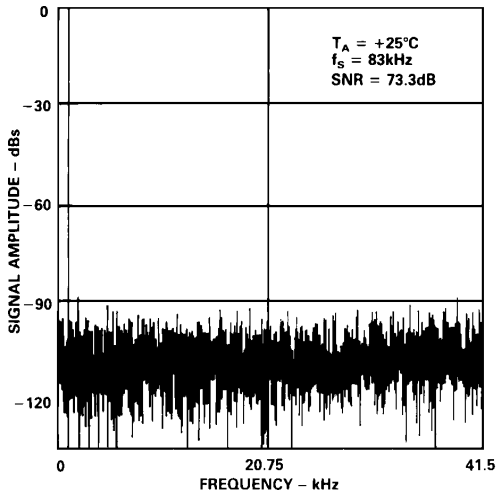


Figure 12. AD7868 DAC FFT Plot

Some applications will require improved performance versus frequency from the AD7868 DAC. In these applications, a simple sample-and-hold circuit such as that outlined in Figure 13 will extend the very good performance of the DAC to 20 kHz. Other applications will already have an inherent sample-and-hold function following the AD7868 DAC output. An example of this type of application is driving a switched-capacitor filter where the updating of the DAC is synchronized with the switched-capacitor filter. This inherent sample-and-hold function also extends the frequency range performance.

Performance versus Frequency

The typical performance plots of Figures 14 and 15 show the AD7868's DAC performance over a wide range of input frequencies at an update rate of 83 kHz. The plot of Figure 14 is without a sample-and-hold on the DAC output while the plot of Figure 15 is generated with a sample-and-hold on the output.

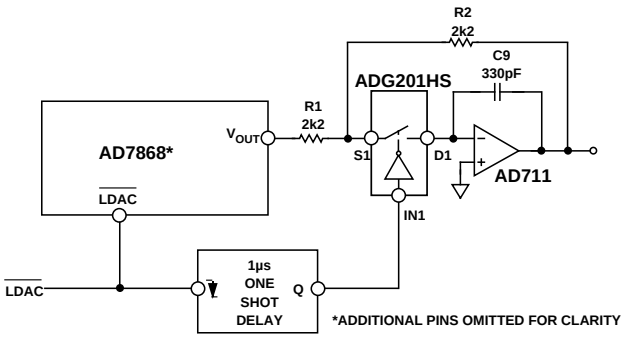


Figure 13. DAC Sample-and-Hold Circuit

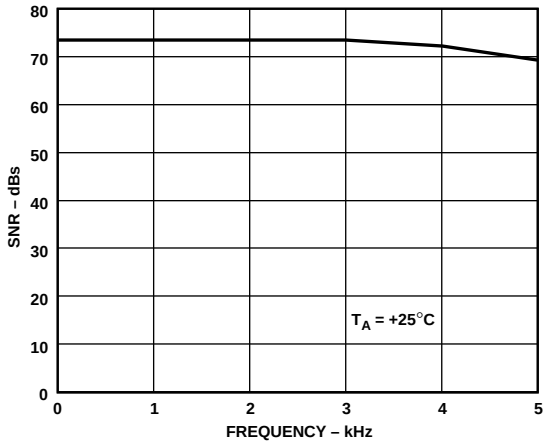


Figure 14. DAC Performance vs. Frequency (No Sample-and-Hold)

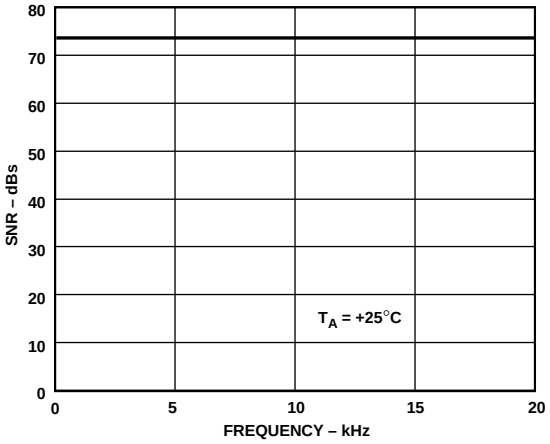


Figure 15. DAC Performance vs. Frequency (Sample-and-Hold)

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD7868 is via a serial bus that uses standard protocol compatible with DSP machines. The communication interface consists of separate transmit (DAC) and receive (ADC) sections whose operations can be either synchronous or asynchronous with respect to each other. Each section has a clock signal, a data signal and a frame or strobe pulse. Synchronous operation means that data is transmitted from the ADC and to the DAC at the same time. In this mode only one interface clock is needed and this has to be the ADC clock out, so RCLK must be connected to TCLK. For asynchronous operation, DAC and ADC data transfers are independent of each other, the ADC provides the receive clock (RCLK) while the transmit clock (TCLK) may be provided by the processor or the ADC or some other external clock source.

Another option to be considered with serial interfacing is the use of a gated clock. A gated clock means that the device that is sending the data switches on the clock when data is ready to be transmitted and three states the clock output when transmission is complete. Only 16 clock pulses are transmitted with the first data bit getting latched into the receiving device on the first falling clock edge. Ideally, there is no need for frame pulses, however, the AD7868 DAC frame input ($\overline{TFS}$) has to be driven high between data transmissions. The easiest method is to use $\overline{RFS}$ to drive $\overline{TFS}$ and use only synchronous interfacing. This avoids the use of interconnects between the processor and AD7868 frame signals. Not all processors have a gated clock facility, Figure 16 shows an example with the DSP56000.

Table I below shows the number of interconnect lines between the processor and the AD7868 for the different interfacing options. The AD7868 has the facility to use different clocks for transmitting and receiving data. This option, however, only exists on some processors and normally just one clock (ADC clock) is used for all communication with the AD7868. For simplicity, all the interface examples in this data sheet use synchronous interfacing and use the ADC clock (RCLK) as an input for the DAC clock (TCLK). For a better understanding of each of these interfaces, consult the relevant processor data sheet.

Table I. Interconnect Lines for Different Interfacing Options

Configuration	No. of Interconnects	Signals
Synchronous	4	RCLK, DR, DT and $\overline{RFS}$ ($TCLK = RCLK$, $\overline{TFS} = \overline{RFS}$)
Asynchronous*	5 or 6	RCLK, DR, $\overline{RFS}$, DT, $\overline{TFS}$ (TCLK = RCLK or µP serial CLK)
Synchronous Gated Clock	3	RCLK, DR and DT ($TCLK = RCLK$, $\overline{TFS} = \overline{RFS}$)

*5 LINES OF INTERCONNECT WHEN TCLK = RCLK
6 LINES OF INTERCONNECT WHEN TCLK = µP SERIAL CLK

AD7868—DSP56000 Interface

Figure 16 shows a typical interface between the AD7868 and DSP56000. The interface arrangement is synchronous with a gated clock requiring only three lines of interconnect. The DSP56000 internal serial control registers have to be configured for a 16-bit data word with valid data on the first falling clock edge. Conversion starts and DAC updating are controlled by an external timer. Data transfers, which occur during ADC conversions, are between the processor receive and transmit shift registers and the AD7868's ADC and DAC. At the end of each 16-bit transfer the DSP56000 receives an internal interrupt indicating the transmit register is empty and the receive register is full.

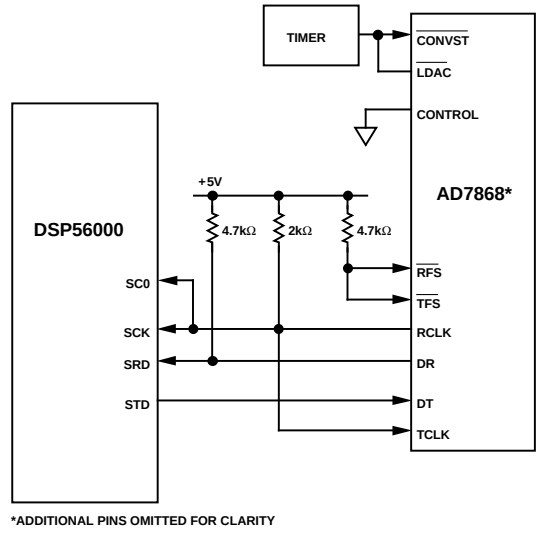


Figure 16. AD7868—DSP56000 Interface

AD7868—ADSP-2101/ADSP-2102 Interface

An interface which is suitable for the ADSP-2101 or the ADSP-2102 is shown in Figure 17. The interface is configured for synchronous, continuous clock operation. The $\overline{LDAC}$ is tied low so the DAC gets updated on the sixteenth falling clock after $\overline{TFS}$ goes low. Alternatively $\overline{LDAC}$ may be driven from a timer as shown in Figure 16. As with the previous interface the processor receives an interrupt after reading or writing to the AD7868 and updates its own internal registers in preparation for the next data transfer.

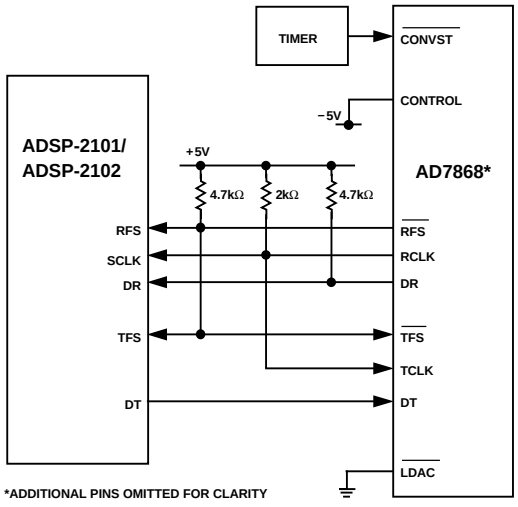


Figure 17. AD7868—ADSP-2101/ADSP-2102 Interface

AD7868—TMS32020/TMS320C25 Interface

Figure 18 shows an interface which is suitable for the TMS32020/TMS320C25 processors. This interface is configured for synchronous, continuous clock operation. Note, the AD7868 will not interface correctly to these processors if the AD7868 is configured for a noncontinuous clock. Conversion starts and DAC updating are controlled by an external timer.

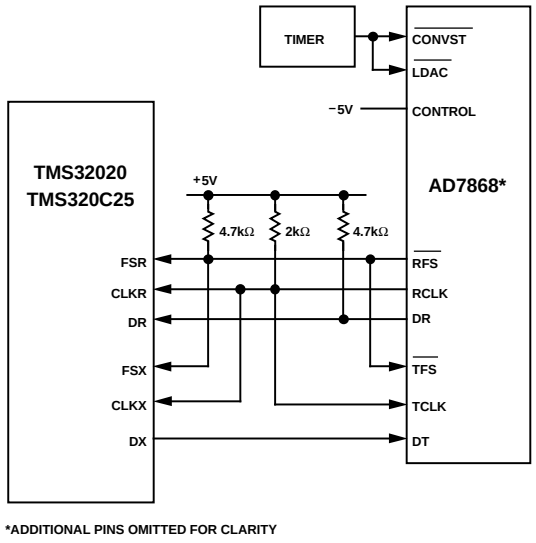


Figure 18. AD7868—TMS32020/TMS320C25 Interface

APPLICATION HINTS

Good printed circuit board (PCB) layout is as important as the circuit design itself in achieving high speed A/D performance. The AD7868's comparator is required to make bit decisions on an LSB size of 1.465 mV. To achieve this, the designer has to be conscious of noise both in the ADC itself and in the preceding analog circuitry. Switching mode power supplies are not recommended as the switching spikes will feed through to the comparator causing noisy code transitions. Other causes of concern are ground loops and digital feedthrough from microprocessors. These are factors which influence any ADC, and a proper PCB layout which minimizes these effects is essential for best performance.

LAYOUT HINTS

Ensure that the layout for the printed circuit board has the digital and analog signal lines separated as much as possible. Take care not to run any digital track alongside an analog signal track. Guard (screen) the analog input with AGND.

Establish a single point analog ground (star ground) separate from the logic system ground as close as possible to the AD7868 AGND pins. Connect all other grounds and the AD7868 DGND to this single analog ground point. Do not connect any other digital grounds to this analog ground point.

Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC, so make the foil width for these tracks as wide as possible. The use of ground planes minimizes impedance paths and also guards the analog circuitry from digital noise. The circuit layout of Figures 22 and 23 have both analog and digital ground planes which are kept separated and only joined together at the AD7868 AGND pins.

NOISE

Keep the input signal leads to V_{IN} and signal return leads from AGND as short as possible to minimize input noise coupling. In applications where this is not possible, use a shielded cable between the source and the ADC. Reduce the ground circuit impedance as much as possible since any potential difference in grounds between the signal source and the ADC appears as an error voltage in series with the input signal.

INPUT/OUTPUT BOARD

Figure 19 shows an analog I/O board based on the AD7868. The corresponding printed circuit board (PCB) layout and silkscreen are shown in Figures 21 to 23.

The analog input to the AD7868 is buffered with an AD711 op amp. There is a component grid provided near the analog input on the PCB which may be used for an antialiasing filter for the ADC or a reconstruction filter for the DAC or any other conditioning circuitry. To facilitate this option, there are two wire links (labeled LK1 and LK2) required on the analog input and output tracks.

The board contains a SHA circuit which can be used on the output of the AD7868 DAC to extend the very good performance of the part over a wider frequency range. The increased performance from the SHA can be seen in Figures 14 and 15 of this data sheet. A wire link (labeled LK3) connects the board output to either the SHA output or directly to the AD7868 DAC output.

There are three $\overline{\text{LDAC}}$ link options on the board; $\overline{\text{LDAC}}$ can be driven from an external source independent of $\overline{\text{CONVST}}$, $\overline{\text{LDAC}}$ can be tied to $\overline{\text{CONVST}}$ or $\overline{\text{LDAC}}$ can be tied to GND. Choosing the latter option of tying $\overline{\text{LDAC}}$ to GND disables the SHA operation, and places the SHA permanently in the track mode.

Microprocessor connections to the board are made by a 9-way D-type connector. The pinout is shown in Figure 20. The ADC's digital outputs are buffered with 74HC4050s. These buffers provide a higher current output capability for high capacitance loads or cables. Normally, these buffers are not required as the AD7868 will be sitting on the same board as the processor.

POWER SUPPLY CONNECTIONS

The PCB requires two analog power supplies and one 5 V digital supply. Connections to the analog supply are made directly to the PCB as shown on the silkscreen in Figure 21. The connections are labeled V+ and V– and the range for both of these supplies is 12 V to 15 V. Connections to the 5 V digital supply are made through the D-type connector SKT6. The ±5 V analog supply required by the AD7868 are generated from two voltage regulators on the V+ and V– supplies.

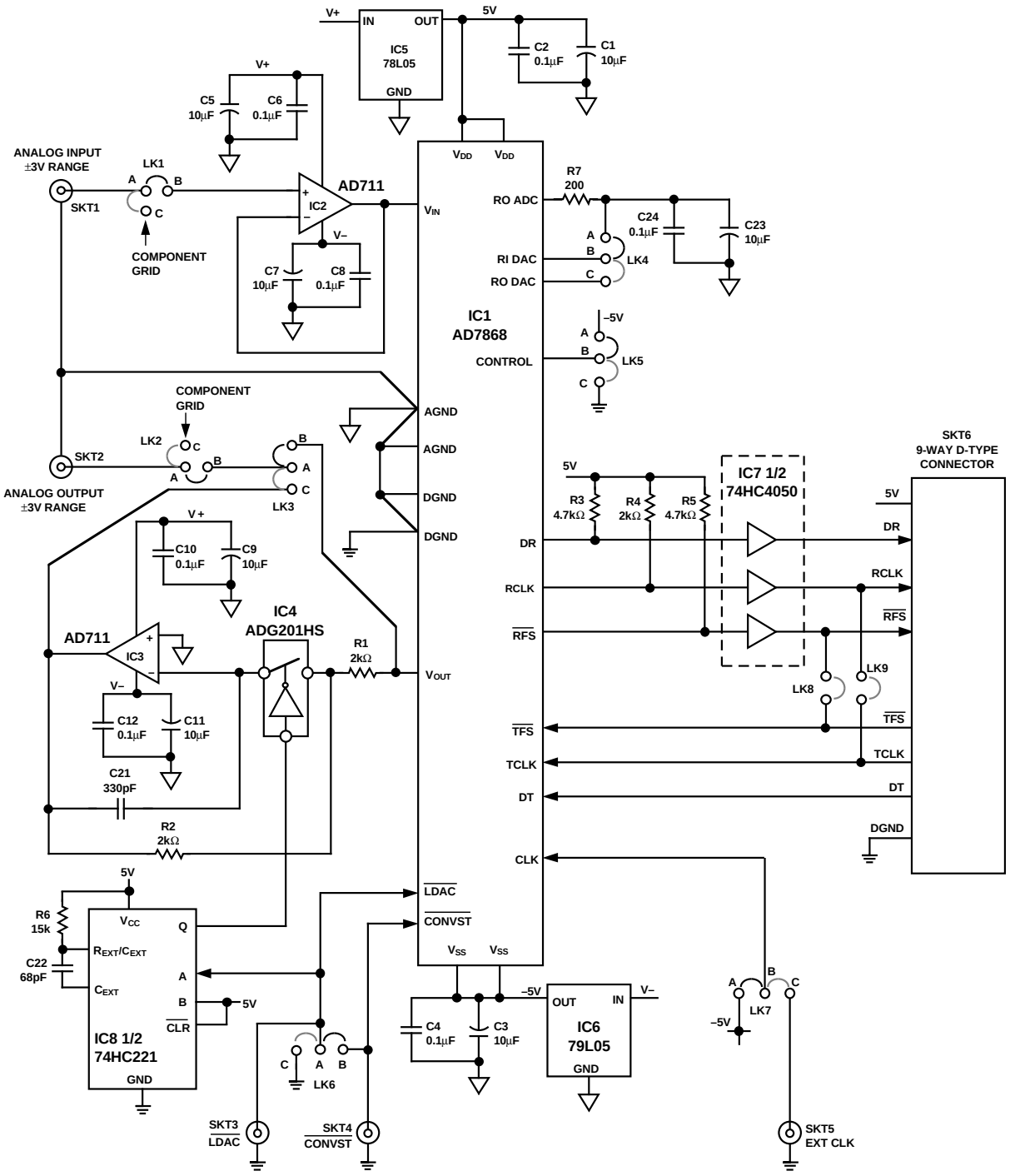


Figure 19. Input/Output Circuit Based on the AD7868

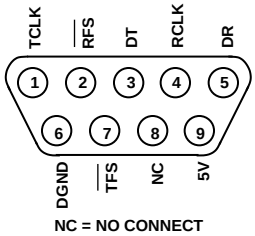


Figure 20. SKT6, D-Type Connector Pinout

WIRE LINK OPTIONS

LK1, Analog Input Link

LK1 connects the analog input to a component grid or to a buffer amplifier which drives the ADC input.

LK2, Analog Output Link

LK2 connects the analog output to the component grid or to either the SHA or DAC output (see LK3).

LK3, SHA or DAC Select

The analog output may be taken directly from the DAC or from a SHA at the output of the DAC.

LK4, DAC Reference Selection
The DAC reference may be connected to either the ADC reference output (RO ADC) or to the DAC reference (RO DAC).

LK5, ADC Internal Clock Selection
This link configures the ADC for continuous or noncontinuous internal clock operation.

LK6, DAC Updating
The DAC, $\overline{\text{LDAC}}$ input may asserted independently of the ADC $\overline{\text{CONVST}}$ signal or it may be tied to $\overline{\text{CONVST}}$ or it may tied to GND.

LK7, ADC Clock Source
This link provides the option for the ADC to use its own internal clock oscillator or an external TTL compatible clock.

LK8 Frame Synchronous Option
LK8 provides the option of tying the ADC $\overline{\text{RFS}}$ output to the DAC $\overline{\text{TFS}}$ input.

LK9 Transmit/Receive Clock Option
LK9 provides the option to connect the ADC RCLK to the DAC TCLK.

COMPONENT LIST

IC1	AD7868
IC2, IC3	2X AD711
IC4,	ADG201HS
IC5,	MC78L05
IC6,	MC79L05
IC7,	74HC4050
IC8,	74HC221
C1, C3, C5, C7 C9, C11, C13, C15 C17, C19, C23	10 µF Capacitor
C2, C4, C6, C8 C10, C12, C14, C16 C18, C20, C24	0.1 µF Capacitor
C21	330 pF Capacitor
C22	68 pF Capacitor
R1, R2, R4	2 kΩ Resistor
R3, R5	4.7 kΩ Resistor
R6	15 kΩ Resistor
R7	200 Ω Resistor
LK1, LK2, LK3, LK4, LK5, LK6, LK7, LK8 LK9	Shorting Plugs
SKT1, SKT2, SKT3, SKT4, SKT5	BNC Sockets
SKT6	9-Contact D-Type Connector

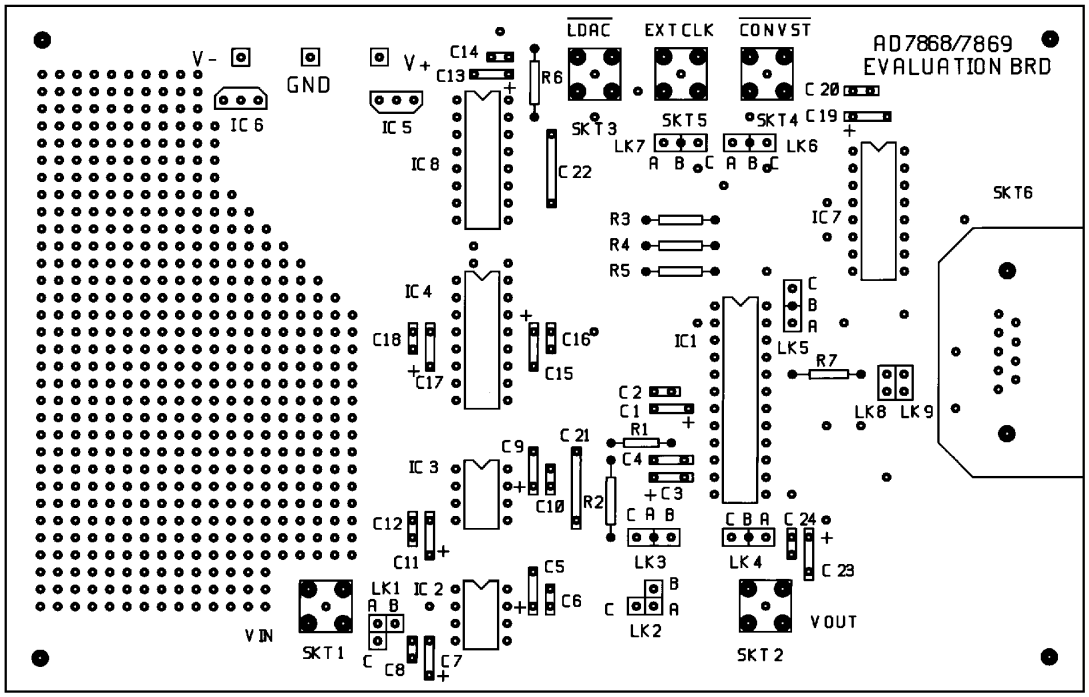


Figure 21. Silkscreen for the Circuit Diagram of Figure 19

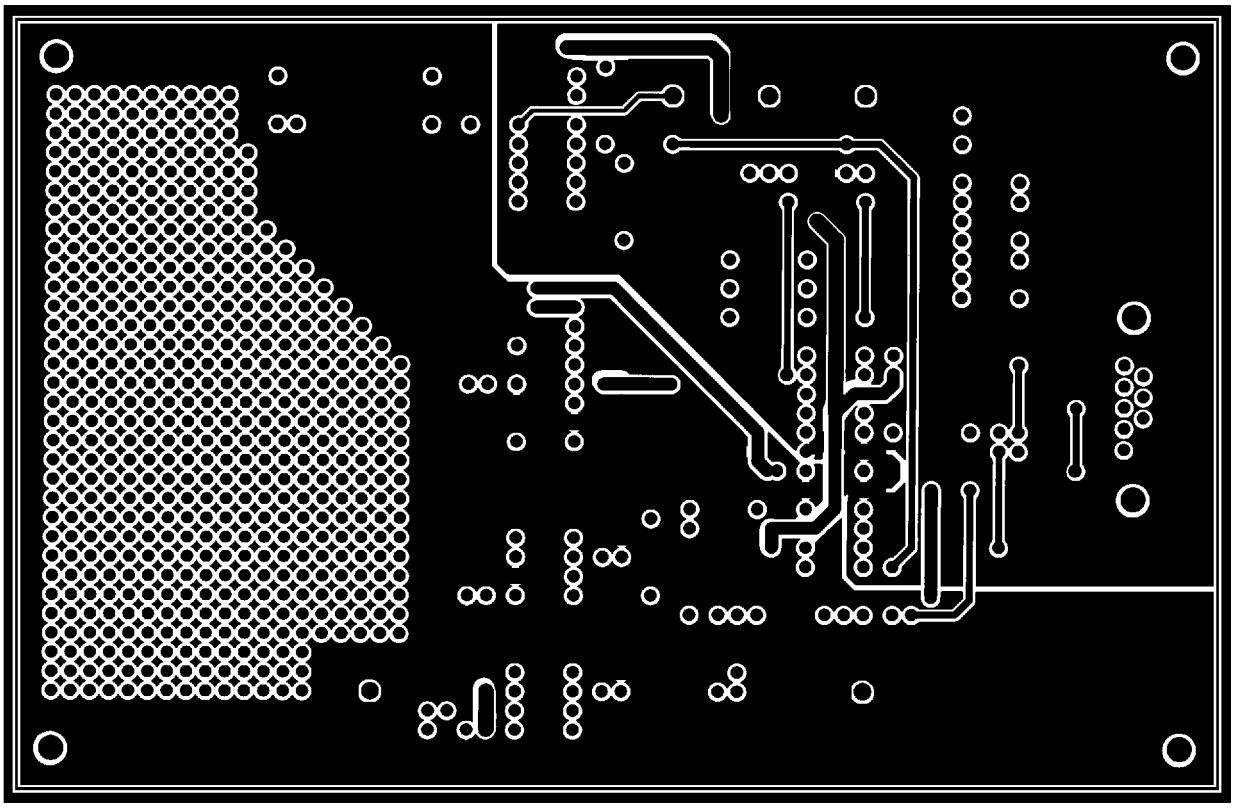


Figure 22. Component Side Layout for the Circuit Diagram of Figure 19

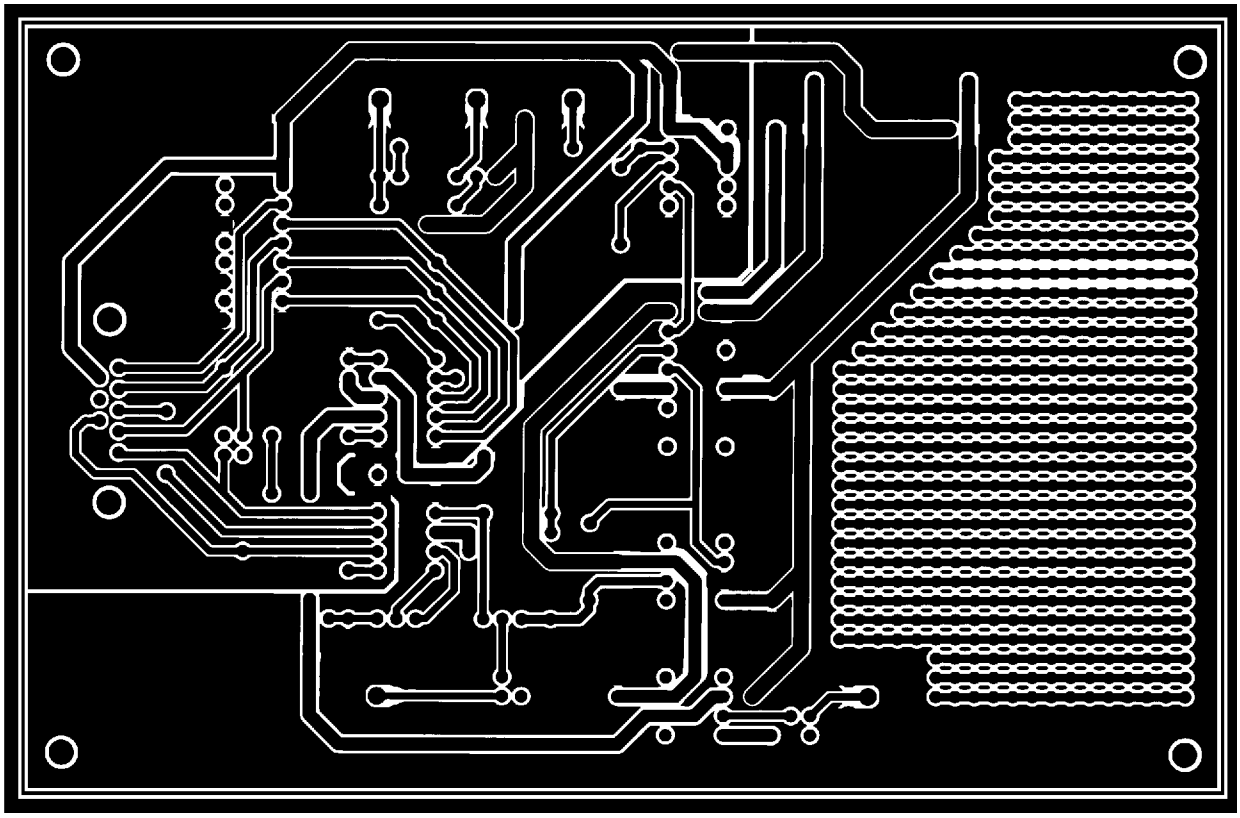
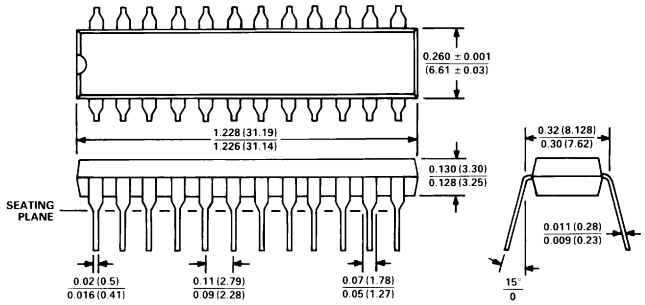


Figure 23. Solder Side Layout for the Circuit Diagram of Figure 19

OUTLINE DIMENSIONS

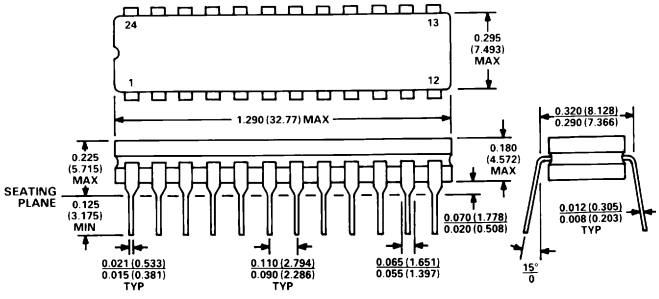
Dimensions shown in inches and (mm).

24-Pin Plastic (N-24)



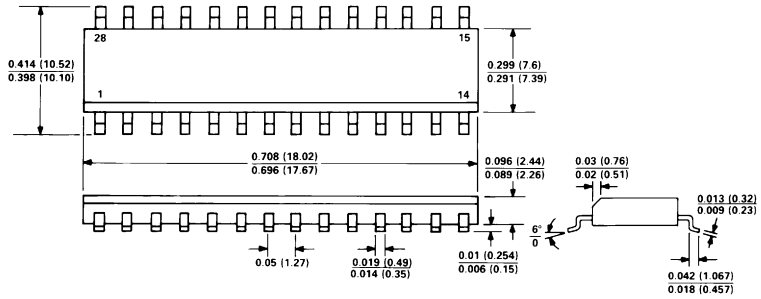
NOTES
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. PLASTIC LEADS WILL BE EITHER SOLDER DIPPED OR TIN LEAD PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

24-Pin Cerdip (Q-24)



1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERDIP LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

28-Pin Plastic SOIC (R-28)



1. LEAD NO. 1 IDENTIFIED BY A DOT.
2. SOIC LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

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